REMARKS

Claims 1-23 were originally filed in the application.

Claims 8-9 and 17-18 were previously cancelled.

Claims 1-7, 10-16 and 19-24 are pending in the application.

Claims 1-7, 10-16 and 19-23 have been rejected.

Claims 1 and 10 have been amended as set forth herein.

Claim 24 is added herein.

Reconsideration of the claims is respectfully requested.

The Applicants have made the arguments set forth above in order to place this Application in condition for allowance. In the alternative, the Applicants have made the amendments and arguments to properly frame the issues for appeal. In this response, the Applicants make no admission concerning any now moot rejection or objection, and affirmatively deny any position, statement or averment of the Examiner that was not specifically addressed herein.

I. CLAIM OBJECTIONS

The claims were objected to because of minor informalities in Claims 1 and 10. Claims 1 and 10 have been amended to correct these informalities. The Applicants respectfully request that the Objections to Claims 1 and 10 be withdrawn.

II. CLAIM REJECTION UNDER 35 U.S.C.§103

Claims 1, 6, 7, 10, 15, 16 and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application Publication No. 2003/0231625 to Calvignac, et al. (hereinafter "*Calvignac*"), in view of U.S. Patent No. 7,415,540 to Fallon, et al. (hereinafter "*Fallon*"), in further view of U.S. Patent Application Publication No. 2006/0104286 to Cheriton (hereinafter "*Cheriton*"). Claims 2, 5, 11, 14, 20 and 23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Calvignac* in view of *Fallon* and *Cheriton*, and in further view of U.S. Patent No. 7,197,035 to Asano (hereinafter "*Asano*"). Claims 3, 4, 12, 13, 21 and 22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Calvignac* in view of *Fallon* and *Cheriton* and in further view of U.S. Patent Application Publication No. 2004/0100956 to Watanabe (hereinafter "*Watanabe*"). Applicants respectfully traverse the rejection.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a prima facie case of obviousness. MPEP § 2142, p. 2100-125 (8th ed. rev. 5, August 2006). Absent such a prima facie case, the Applicants are under no obligation to produce evidence of nonobviousness. *Id.* To establish a *prima facie* case of obviousness, three basic criteria must be met: *Id.* First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. *Id.* Second, there must be a reasonable expectation of success. *Id.* Finally, the prior art reference (or references when combined) must teach or suggest all the claim

limitations. *Id.* The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure. *Id.*

Claim 1 recites the unique and non-obvious limitations emphasized below:

> 1. A router for interconnecting external devices coupled to said router, said router comprising:
> a switch fabric; and
> a plurality of routing nodes coupled to said switch fabric, wherein each of said plurality of routing nodes comprises:
> a first network processor comprising a first plurality of microengines, each of said first plurality of microengines for performing first security and classification functions associated with data packets received from said external devices and transmitted to said switch fabric, wherein each data packet is distributed to a selected microengine;
> a second network processor comprising a second plurality of microengines, each of said second plurality of microengines for performing second security and classification functions associated with data packets received from said switch fabric and transmitted to said external devices, wherein each data packet is distributed to a selected microengine; and
> a routing table search circuit comprising an initial content addressable memory stage followed by a plurality of trie tree search table stages, wherein one of said first and second security and classification functions is performed according to information from the routing table search circuit. [Emphasis Added]

Applicants submit that *Calvignac*, *Fallon*, and *Cheriton*, either alone or in combination, do not teach or suggest the above-emphasized limitation of Claim 1. In particular, it is submitted that *Cheriton* fails to remedy the conceded deficiencies of *Calvignac* and *Fallon*. Accordingly, without

conceding the propriety of the asserted combination, the asserted combination of *Calvignac*, *Fallon*, and *Cheriton* likewise is deficient.

In rejecting Claim 1, the Office Action acknowledged that the combination of *Calvignac* and *Fallon* does not disclose a routing node that comprises "a routing table search circuit comprising an initial content addressable memory stage followed by a plurality of trie tree search table stages, wherein one of said first and second security and classification functions is performed according to information from the routing table search circuit." (Office Action, page 7). However, the Office Action asserted that *Cheriton* discloses the aforementioned routing table search circuit, citing Figure 2A and paragraph [0021] of *Cheriton* for support.

The Office Action is incorrect because *Cheriton* does not teach a routing table search circuit comprising an initial content addressable memory (CAM) stage followed by a plurality of trie tree search table stages. Figure 2A of *Cheriton*, which is a block diagram of a packet classifier, shows one or more ternary content addressable memories (TCAMs) 203 followed by one or more binary addressable memories (e.g., CAMs, hash table, tries) 204. CAMs are distinguishable from TCAMs in that CAMs utilize binary logic (e.g., 1s and 0s) whereas TCAMs allow a third matching state (e.g., "X" or "Don't Care"). Furthermore, *Cheriton* acknowledges this distinction in Figure 2A by specifying that TCAMs are followed by one or more binary addressable memories and naming CAMs as an example of such. Moreover, *Cheriton* expresses whether a CAM is binary or ternary throughout the disclosure, including in paragraph [0021]. In fact, *Cheriton* teaches away from having a CAM stage followed by a trie tree search stage by discussing the reason for utilizing a

TCAM over a binary CAM. See *Cheriton*, paragraph [0020]. As TCAMs are not the same as CAMs, a set of TCAMs followed by a set of binary addressable memories (as taught by *Cheriton*) is not the same as "a routing table search circuit comprising an initial content addressable memory stage followed by a plurality of trie tree search table stages," as recited in Claim 1.

Additionally, *Cheriton* also does not teach or suggest security and classification functions being performed according to information from the routing table search circuit. Applicants have already demonstrated that *Cheriton* does not teach a routing table circuit comprising an initial content addressable memory stage followed by a plurality of trie tree search table stages. Therefore, *Cheriton* logically cannot teach or suggest any security and classification functions that are performed according to information from the routing table search circuit of Claim 1. Consequently, *Cheriton* fails to teach or suggest "a routing table search circuit comprising an initial content addressable memory stage followed by a plurality of trie tree search table stages, wherein one of said first and second security and classification functions is performed according to information from the routing table search circuit." Accordingly, *Cheriton* does not remedy the conceded deficiencies of *Calvignac* and *Fallon*. Applicants respectfully request that the § 103 rejection with respect to Claim 1 and its dependent claims be withdrawn.

Independent Claims 10 and 19 recite limitations analogous to limitations recited in Claim 1. Therefore, Claims 10 and 19 are allowable for the same or similar reasons as Claim 1. Accordingly, Applicants respectfully request that the § 103 rejection with respect to claims 10 and 19 and their dependents be withdrawn.

Applicants respectfully disagree with the Office Action's rejections of Claims 1-7, 10-16 and 19-23 based on additional erroneous interpretations or misapplications of *Calvignac*, *Fallon*, *Cheriton*, *Asano*, and *Watanabe* to at least some of Claims 1-7, 10-16 and 19-23. However, Applicants' arguments regarding those other shortcomings of *Calvignac*, *Fallon*, *Cheriton*, *Asano*, and *Watanabe* are moot in view of the arguments above. Applicants reserve the right to dispute in future responses to Office Actions the appropriateness and application of *Calvignac*, *Fallon*, *Cheriton*, *Asano*, and *Watanabe* to the claims of the present application, including the right to dispute the assertions made in the September 17, 2009 Office Action.

III. NEW CLAIMS

The Applicants have added new Claim 24. The Applicants respectfully submit that no new matter has been added. At a minimum, the Applicants respectfully submit that Claim 24 is patentable for one or more reasons discussed above. The Applicants respectfully request entry and full allowance of Claim 24.

CONCLUSION

As a result of the foregoing, the Applicants assert that the remaining claims in the Application are in condition for allowance, and respectfully requests that this Application be passed to issue.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at ***jmockler@munckcarter.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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